What is claimed is

1. A method of erasing a non-volatile semiconductor memory device having a memory transistor comprising a source region and a drain region formed on a surface portion of a semiconductor while sandwiching a channel-forming region there between, a gate insulating film provided on the channel-forming region and including dispersed charge storing means, and a gate electrode on the gate insulating film,

said method comprising the steps of repeating a write-erase operation a plurality of times when erasing the memory transistor.

2. A method of erasing a non-volatile semiconductor memory device having a memory transistor comprising a source region and a drain region formed on a surface portion of a semiconductor while sandwiching a channel-forming region there between, a gate insulating film provided on the channel-forming region and including dispersed charge storing means, and a gate electrode on the gate insulating film,

said method comprising, when erasing the memory transistor, the steps of:

performing an erase operation; and

performing a write-erase operation at least once.

3. A method of erasing a non-volatile semiconductor memory device having a memory transistor comprising a source region and a drain region formed on a surface portion of a semiconductor while sandwiching a channel-forming region there between, a gate insulating film provided on the channel-forming region and including dispersed charge storing means, and a gate electrode on the gate insulating film,

the method comprising, when erasing the memory transistor, the steps of:

performing a write operation; and

performing an erase operation.

4. A method of erasing a non-volatile semiconductor memory device as set forth in claim 1, wherein said memory device comprises:

a plurality of memory transistors arranged in a bit direction and a word direction;

a plurality of word lines;

a plurality of common lines in the bit direction intersecting the plurality of word lines in an electrically insulated state;

a plurality of the gate electrodes connected to the plurality of word lines; and

a plurality of said source regions or drain regions coupled to said plurality of common lines.

5. A method of reading a non-volatile semiconductor memory device as set forth in claim 4, wherein said memory device comprises:

a word line for commonly connecting said gate electrodes in the word direction;

a source line for commonly connecting said source regions in the bit direction; and

a bit line for commonly connecting said drain regions in the bit direction.

6. A method of erasing a non-volatile semiconductor memory device as set forth in claim 5, wherein: in said memory device,

said source line comprises a sub source line for commonly connecting said source regions in the bit direction, and a main source line for commonly connecting sub source lines in the bit direction; and

said bit line comprises a sub bit line commonly connecting said drain regions in the bit direction, and a main bit line for commonly connecting sub bit lines in the bit direction.

7. A method of reading a non-volatile semiconductor memory device as set forth in claim 1, wherein said memory device comprises the dispersed charge storing means made to be separated at least a surface direction facing said channel-forming region.

8. A method of erasing a non-volatile semiconductor memory device as set forth in claim 1, wherein said memory device comprises the dispersed charge storing means does not have conductivity over an entire surface direction facing said channel-forming region at least when charges do not dissipate outside.

9. A method of erasing a non-volatile semiconductor memory device as set forth in claim 8. wherein said gate insulating film includes:

a tunnel insulating film on said channel-forming region; and

a nitride film or an oxynitride film on the tunnel insulating film.

10. A method of erasing a non-volatile semiconductor memory device as set forth in claim 8, wherein said gate insulating film includes:

a tunnel insulating film on said channel-forming region; and

mutually insulated fine particle conductors formed on the tunnel insulating film as the above dispersed charge storing means.

11. A method of erasing a non-volatile semiconductor memory device as set forth in claim 10, wherein said fine particle conductors have a particle diameter of not more than 10 nm.

12. A method of erasing a non-volatile semiconductor memory device having a memory transistor comprising a source region and a drain region formed on a surface portion of a semiconductor while sandwiching a channel-forming region there between, a gate insulating film provided on the channel-forming region and including dispersed charge storing means, and a gate electrode on the gate insulating film,

said method comprising the steps of:

setting an erasure voltage and/or erasure time corresponding to the phenomenon of an absolute value of the voltage of an inflection point taking an extremum at the erasing side in a hysteresis curve of change shown the threshold voltage with respect to the applied voltage of said memory transistor becoming larger along with shortening of the voltage application time; and

erasing said memory transistor by using that erasure voltage and/or erasure time.

13. A method of erasing a non-volatile semiconductor memory device as set forth in claim 12, comprising the steps of:

setting the erasure voltage within a range not exceeding the voltage of said inflection point in absolute value; and

erasing said memory transistor using the set

erasure voltage and corresponding erasure time.

14. A method of erasing a non-volatile semiconductor memory device as set forth in claim 13, comprising the steps of:

setting said erasure voltage at the same value as the voltage of said inflection point or between the voltage of the inflection point and the minimum voltage for generating an electric field required for causing said charge storing means to become saturated.

15. A method of erasing a non-volatile semiconductor memory device having a memory transistor comprising a source region and a drain region formed on a surface portion of a semiconductor while sandwiching a channel-forming region there between, a gate insulating film provided on the channel-forming region and including dispersed charge storing means, and a gate electrode on the gate insulating film,

said method comprising the steps of:

setting the erasure voltage the same as the voltage of the inflection point taking an extremum at the erasing side in the hysteresis curve shown the change of threshold voltage with respect to the applied voltage of said memory transistor or between the voltage of the inflection point and the minimum voltage for generating the electric field required for causing said dispersed

charge storing means to become saturated; and

erasing said memory transistor using the erasure voltage.

16. A method of erasing a non-volatile semiconductor memory device having a memory transistor comprising a source region and a drain region formed on a surface portion of a semiconductor while sandwiching a channel-forming region there between, a gate insulating film provided on the channel-forming region and including dispersed charge storing means, and a gate electrode on the gate insulating film,

said method comprising, in a single erasure operation of said memory transistor, the steps of:

performing a plurality of erase operations including an erase operation using an erasure voltage the same as or smaller than, in absolute value, the voltage of the inflection point taking an extremum at the erasing side in a hysteresis curve shown the change of threshold voltage with respect to the applied voltage of the memory transistor while changing the erasure voltage and the erasure time.

17. A method of erasing a non-volatile semiconductor memory device as set forth in claim 16, further comprising the step of:

repeating erase and write operations a

plurality of times in the above single erasure operation.

18. A method of erasing a non-volatile semiconductor memory device as set forth in claim 16, further comprising the steps of:

performing an erase operation once; and

performing a write-erase operation at least once in the above single erasure operation.

19. A method of erasing a non-volatile semiconductor memory device as set forth in claim 16, further comprising the steps of:

performing a write operation; and

performing erase operation in the above single erasure operation.

20. A method of erasing a non-volatile semiconductor memory device as set forth in claim 16, further comprising the step of:

erasing by using an erasure voltage of a larger absolute value than the voltage of the inflection point in the above single erasure operation.

21. A method of erasing a non-volatile semiconductor memory device as set forth in claim 16, further comprising the step of:

setting the erasure voltage and the erasure time in accordance with the phenomenon of the voltage of the inflection point shifting to the negative side along

with a shortening of the voltage application time.

22. A method of erasing a non-volatile semiconductor memory device as set forth in claim 12, wherein said memory device comprises:

a plurality of memory devices arranged in a bit direction and a word direction;

a plurality of word lines;

a plurality of common lines in the bit direction intersecting the plurality of word lines in an electrically insulated state;

a plurality of said gate electrodes connected to said plurality of word lines; and

a plurality of said source regions or drain regions coupled to said plurality of common lines.

23. A method of reading a non-volatile semiconductor memory device as set forth in claim 22, wherein said memory device comprises:

a word line for commonly connecting said gate electrodes in the word direction;

a source line for commonly connecting said source regions in the bit direction; and

a bit line for commonly connecting said drain regions in the bit direction.

24. A method of erasing a non-volatile semiconductor memory device as set forth in claim 23,

wherein:

said source line comprises a sub source line for commonly connecting said source regions in the bit direction, and a main source line for commonly connecting sub source lines in the bit direction; and

said bit line comprises a sub bit line commonly connecting said drain regions in the bit direction, and a main bit line for commonly connecting sub bit lines in the bit direction.

25. A method of reading a non-volatile semiconductor memory device as set forth in claim 12, wherein said memory device comprises the dispersed charge storing means made to be separated at least in a surface direction facing said channel-forming region.

26. A method of erasing a non-volatile semiconductor memory device as set forth in claim 12, wherein said memory device comprises the dispersed charge storing means does not have conductivity over an entire surface direction facing said channel-forming region at least when charges do not dissipate outside.

27. A method of erasing a non-volatile semiconductor memory device as set forth in claim 26, wherein said gate insulating film includes:

a tunnel insulating film on said channel-forming region; and

a nitride film or an oxynitride film on the tunnel insulating film.

28. A method of erasing a non-volatile semiconductor memory device as set forth in claim 26, wherein said gate insulating film includes:

a tunnel insulating film on said channel-forming region; and

mutually insulated fine particle conductors formed on the tunnel insulating film as the above dispersed charge storing means.

29. A method of erasing a non-volatile semiconductor memory device as set forth in claim 28, wherein said fine particle conductors have a particle diameter of not more than 10 nm.

30. A non-volatile semiconductor memory device having a memory transistor comprising a source region and a drain region formed on a surface portion of a semiconductor while sandwiching a channel-forming region there between, a gate insulating film comprised of a tunnel insulating film, a nitride film, and a top insulating film sequentially stacked on the channel-forming region and including dispersed charge storing means in the stacked films, and a gate electrode on the gate insulating film, wherein

thicknesses of said tunnel insulating film and

said top insulating film are set so that the thickness of said gate insulating film converted to an oxide film becomes 10 nm or less and the change of the threshold voltage at the time of erasing said memory transistor is regulated by a recombination process of a hole current injected from said channel-forming region side and an electron current injected from said gate electrode side.

31. A non-volatile semiconductor memory device as set forth in claim 30, wherein

the thickness of said tunnel insulating film is 2.5 nm or more, and

a ratio of thickness of the top insulating film to said tunnel insulating film is 1.4 or more.

32. A non-volatile semiconductor memory device as set forth in claim 30, further comprising:

a plurality of word lines;

a plurality of common lines in the bit direction intersecting the plurality of word lines in an electrically insulated state;

a plurality of gate electrodes connected to the plurality of word lines; and

a plurality of said source regions or drain regions coupled to said plurality of common lines.

33. A non-volatile semiconductor memory device as set forth in claim 32, comprising:

a word line for commonly connecting said gate electrodes in the word direction;

a source line for commonly connecting said source regions in the bit direction; and

a bit line for commonly connecting said drain regions in the bit direction.

34. A non-volatile semiconductor memory device as set forth in claim 33, wherein

said source line comprises a sub source line for commonly connecting said source regions in the bit direction, and a main source line for commonly connecting sub source lines in the bit direction; and

said bit line comprises a sub bit line commonly connecting said drain regions in the bit direction, and a main bit line for commonly connecting sub bit lines in the bit direction.

35. A non-volatile semiconductor memory device as set forth in claim 30, wherein said dispersed charge storing means is made to be separated at least in a surface direction facing said channel-forming region.

36. A non-volatile semiconductor memory device as set forth in claim 30, wherein said dispersed charge storing means does not have conductivity over the entire surface direction facing said channel-forming region at least when charges do not dissipat outside.

37. A non-volatile semiconductor memory device as set forth in claim 36, wherein said gate insulating film includes:

a tunnel insulating film on said channel forming region; and

a nitride film or an oxynitride film on the tunnel insulating film.

38. A non-volatile semiconductor memory device as set forth in claim 36, wherein said gate insulating film includes:

a tunnel insulating film on said channel-forming region; and

mutually insulated fine particle conductors formed on the tunnel insulating film as the above dispersed charge storing means.

39. A non-volatile semiconductor memory device as set forth in claim 38, wherein said fine particle conductors have a particle diameter of not more than 10 nm.